New Resonant Inverter Tuning for Three-Phase Current Source Parallel Resonant Inverters

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Abstract: This paper presents a new tuningloop for three-phase current source parallel resonant inverters. The switching frequency is tuned by using a phase-locked loop (PLL) circuit based on a new Phase Detector (PD). In practice, the resonant capacitors and inductors have tolerances that cause different resonant frequency for each phase. This paper shows that a conventional PDcauseshigher voltage stress over switches and DC-link inductor. In the proposed tuning loop, the PLL tracks the average value of the resonant frequencies that reduces the voltage stress. In addition, there is no feedback from the loadcurrents to detect the phase error, which is another advantage of the new method. A laboratory prototype of a three-phase current source parallel resonant half-bridge inverter was built to verify the advantages of the proposed tuning system with operating frequency of 22 kHz.

Keywords: resonant inverter tuning; three-phase current source parallel resonant inverters; phase-locked loop (PLL)

1 Introduction

Resonant Inverters are most commonly used because they provide sinusoidal waveforms with lower harmonics and less EMI problems. A large number of topologies have been developed in this area which can be divided into single-phase and multi-phase structures. Three-phase resonant inverters are widely used in industrial applications. Such applications include high power DC-DC converters, contact-less power transfer systems and multi-phase induction heating systems [1-13].

In comparison with single-phase resonant inverters, the three-phase inverters have a smaller input filter and higher power density. Moreover, the load currents and output voltages have less distortion due to third order harmonics elimination for three-wire structures. Hence, the three-phase resonant inverters have better sinusoidal waveforms in low quality factors (Q<5) which is important in traveling wave induction heating systems [9].

Three-phase current-fed parallel resonant inverters are widely utilized in high voltage and high power DC-DC converters; because they provide higher boosting ratio and they have no current sharing problems. The current source inverters have limited control methods but they are less affected by input voltage ripples and they have short-circuited protection capability [13-20]. Figure 1 shows two possible topologies for three-phase current source parallel resonant inverters with three-wire connection.

Conventionally, PDs measure the phase difference between the voltage and the current of a single resonant tank [21-25]. Hence, a conventional PLL is applicable when the three resonant tanks have a same resonant frequency. However, designing the three resonant tanks without tolerance and frequency deviation is practically impossible. This paper shows that the three-phase current source topologies are sensitive to the tolerances and the systems are unbalanced under no-load and light-load conditions. In addition, the switching losses, DC-link current ripples and voltage stress are increased. The proposed PD tracks the average value of the resonant frequencies that reduces the DC-link current ripples and voltage stress over the switches S_1-S_6.

In a conventional tuning loop, the current of resonant tank is measured for phase error detection. In the new PLL, voltages of the low-side switches are the inputs of the PD and there is no feedback from the output currents. Thus, there is no Current Transformer (CT) or Hall Effect sensor for current sensing, which makes the system simple, more reliable and cost effective. The dynamic behavior of the new tuning loop is simulated in steady state and transient conditions. The proposed PD has similar structure for the two topologies, as shown in Figure 1. For simplicity, the laboratory prototype is implemented based on the half-bridge inverter.

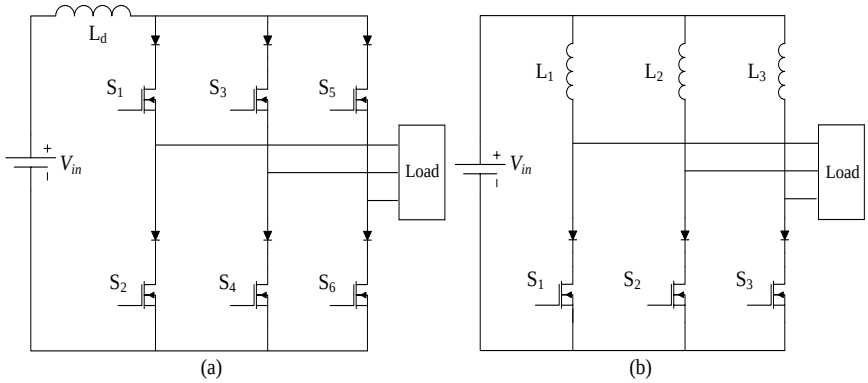


Figure 1

Three-phase current source parallel resonant topologies: (a) the full-bridge inverter; (b) the half-bridge inverter

2 System Description

Figure 2 shows the half-bridge topology with a star-connected resonant tank. The performance of the resonant inverter tuning is similar for the half-bridge and full-bridge inverters. In the both cases, each switch conducts 120 degrees to achieve Zero Voltage and Zero Current Switching (ZVZCS) at the resonant frequency. The half-bridge inverter has asymmetrical current injection while the full-bridge inverter has symmetrical current injection.

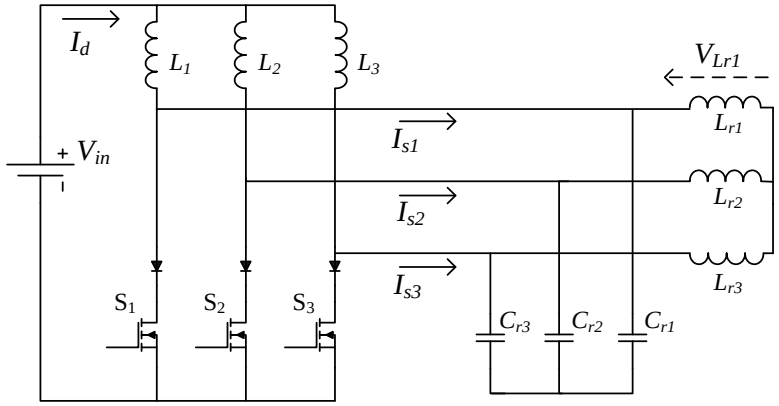


Figure 2
The half-bridge inverter with star-connected resonant tank

Figure 3 shows the three-step operation of the half-bridge inverter where each switch conducts for 120 degrees of the switching period. Each switch is connected in series with a blocking diode to prevent the internal body diode of the switches from short circuit. Operation of the inverters is investigated with and without the tolerances as follows:

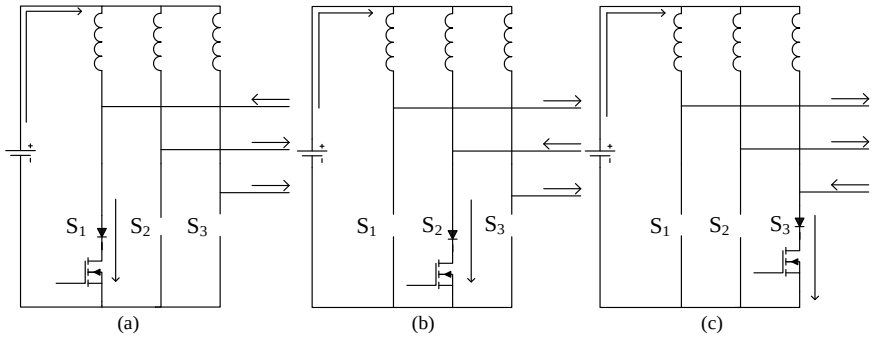


Figure 3
Three-step operation of the half bridge inverter

2.1 Operation without the Tolerances

In this section, the parameters of the inverter are considered with no tolerance. Hence, the three resonant tanks have a similar resonant frequency. The inductance of L_1, L_2 and L_3 (L_d for full-bridge inverter as seen from Figure 1) are much larger than the resonant inductors ($L_{r1} = L_{r2} = L_{r3} = L_r$), so under normal steady state operation the DC-link current, I_d, is approximately constant.

Regarding Figure 3, voltage of S_1 is derived by equation (1) for a switching period duration while the converter works at the resonant frequency. The ω_r, T_s, C_r and V_m are the angular resonant frequency, switching period, per-phase resonant capacitor and phase-phase voltage of the inverter.

$$\begin{aligned} &V_{S1} = 0, && 0 < t < \frac{T_s}{3} \\ &V_{S1} = V_m sin(\omega_r t - \frac{2\pi}{3}), && \frac{T_s}{3} < t < \frac{2T_s}{3} \quad , \ \omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \\ &V_{S1} = -V_m sin(\omega_r t), && \frac{2T_s}{3} < t < T_s \end{aligned} \tag{1}$$

For the half-bridge inverters, the amplitude of the phase-phase voltage, V_m, is derived by employing the inductor volt-second balance principle on L_1, where V_{in} is the DC-link voltage. Similarly, V_m is derived by equation (3) for the full-bridge inverters by employing the inductor volt-second balance principle on L_d.

$$\int_0^{2\pi} V_{L1} d\theta = \int_0^{\frac{2\pi}{3}} V_{in} d\theta + \int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} [V_{in} - V_m sin(\theta - \frac{2\pi}{3})] d\theta + \int_{\frac{4\pi}{3}}^{2\pi} [V_{in} + V_m sin(\theta)] d\theta = 0 \tag{2}$$

$$\rightarrow V_m = \frac{2\pi}{3} V_{in}$$

$$V_m = \frac{\pi}{3} V_{in} \tag{3}$$

Figure 4 shows per-phase equivalent circuit of the resonant inverter and R is the per-phase load resistance. According to 120^0 conduction, the I_{s1} and voltage of S_1 are shown in Figure 5 for the full-bridge and half bridge topologies at the resonant frequency. For the both topologies, the peak voltage of the switches is the amplitude of the phase-phase voltage or V_m. The DC-link voltage, V_{in}, of the two topologies is 50 V. As seen from Figure 5(b), the injected current of the full-bridge inverter has no third order harmonics. Hence, the inverter have lower THD of current for low quality factor operations (Q<5), in comparison with single-phase topologies [14-20].

The quality factor of the parallel resonant load is derived by equation (4). For the half-bridge topology, the injected current has second order harmonics and is suitable for high quality factor operations. In addition, the half-bridge topology is useful for high boosting ratio converters, as shown in equation (2).

$$Q = \frac{R}{\omega_r L_r} \tag{4}$$

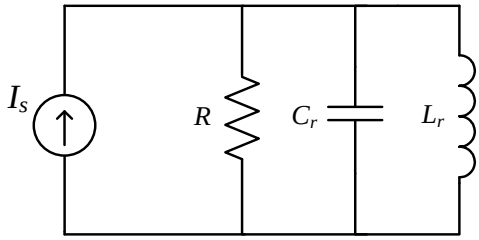


Figure 4
Single-phase equivalent circuit of the resonant tank and the inverter

Let's consider that the switching frequency of the inverter is greater (or smaller) than the resonant frequency. Hence, there is a phase difference, β, between the injected current, I_s, and voltage of the tank circuit. Figure 6 shows the phase plot of a parallel resonant tank with quality factor of10 and resonant frequency of 25 kHz. The phase plot represents the phase difference β between the injected current I_s and the resonant tank voltage for different switching frequencies.

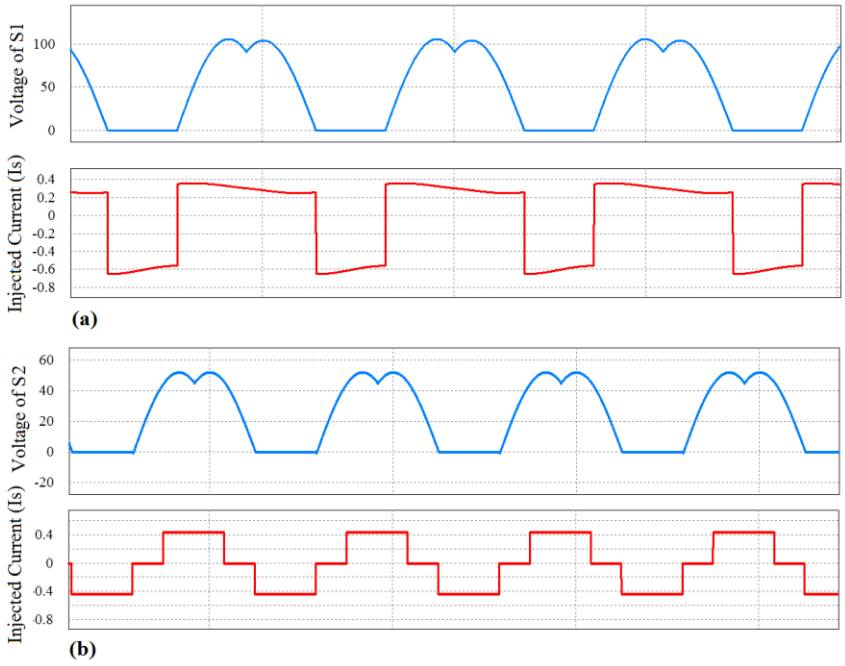


Figure 5
The voltage of S_1 and the injected current connected to S_1, I_{s1}: (a) for the half-bridge inverter; (b) voltage for the full-bridge inverter

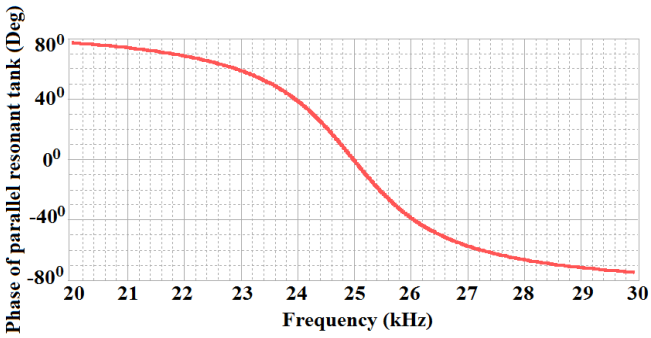


Figure 6

Phase plot of a parallel resonant tank with quality factor of 10

Figure 7 shows the voltage of S_1 and the phase difference β for two conditions (over and under the resonant frequency). Regarding equation (2), the peak value of the phase-phase voltage, V_m, is rewritten as follows:

$$\int_0^{2\pi} V_{L1}d\theta = \int_0^{\frac{2\pi}{3}} V_{in}d\theta + \int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} [V_{in} - V_m \sin(\theta - \frac{2\pi}{3} + \beta)]d\theta + \int_{\frac{4\pi}{3}}^{2\pi} [V_{in} + V_m \sin(\theta + \beta)]d\theta = 0 \quad (5)$$

$$\rightarrow V_m = \frac{2\pi}{3\cos\beta} V_{in}$$

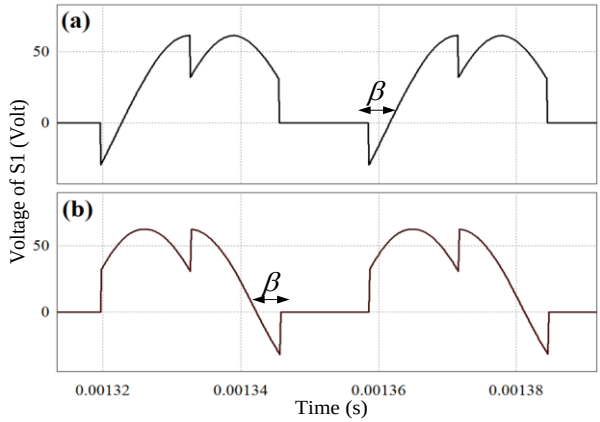


Figure 7

Voltage of S_1 at the two different conditions: (a) over the resonant frequency; (b) under the resonant frequency

Forthe full-bridge topology, the equation (5) is rewritten as follows:

$$\rightarrow V_m = \frac{\pi}{3\cos\beta} V_{in}$$

2.2 Operation with the Tolerances

Let's consider that each resonant tank has different parameters (different L_r and C_r). Hence, the frequency deviation Δf caused by the tolerances is derived as follows:

$$\Delta f = \frac{\partial f_r}{\partial L_r}\Delta L_r + \frac{\partial f_r}{\partial C_r}\Delta C_r = -\frac{1}{4\pi\sqrt{L_r C_r}}\left(\frac{\Delta L_r}{L_r} + \frac{\Delta C_r}{C_r}\right) \Rightarrow \Delta f = -\frac{f_r}{2}\left(\frac{\Delta L_r}{L_r} + \frac{\Delta C_r}{C_r}\right) \tag{6}$$

Figure 8(a) and Figure 8(b) show the phase plot of the three parallel resonant tanks with quality factors of 10 and 2, respectively. The frequency deviations for the resonant tanks1 to 3 are assumed to be 0%, +3% and -3%, respectively. The average value of the three resonant frequencies (f_{r1}, f_{r2} and f_{r3}) is 25 kHz.

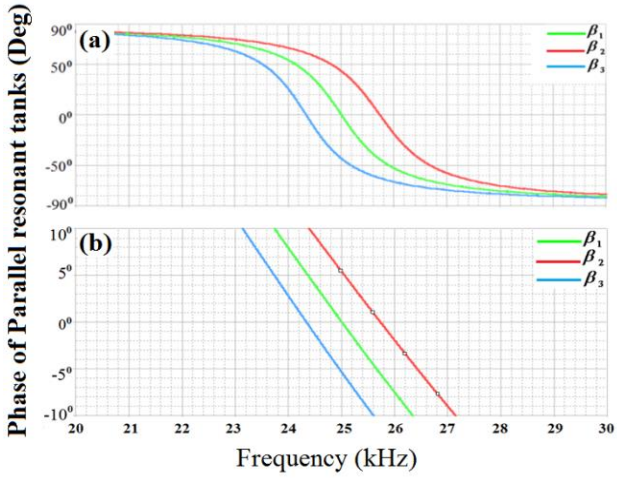


Figure 8

The phase plot of three parallel resonant tanks: (a) quality factor of 10; (b) quality factor of 2

According to equation (2), the phase-phase voltages of the resonant tanks are derived by solving the equations (7) through (9):

$$\int_0^{2\pi} V_{L1}d\theta = \int_0^{\frac{2\pi}{3}} V_{in}d\theta + \int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} [V_{in} - V_{m2}\sin(\theta - \frac{2\pi}{3} + \beta_2)]d\theta + \int_{\frac{4\pi}{3}}^{2\pi} [V_{in} + V_{m3}\sin(\theta + \beta_3)]d\theta = 0 \tag{7}$$

$$\int_0^{2\pi} V_{L2}d\theta = \int_0^{\frac{2\pi}{3}} V_{in}d\theta + \int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} [V_{in} - V_{m3}\sin(\theta - \frac{2\pi}{3} + \beta_3)]d\theta + \int_{\frac{4\pi}{3}}^{2\pi} [V_{in} + V_{m1}\sin(\theta + \beta_1)]d\theta = 0 \tag{8}$$

$$\int_0^{2\pi} V_{L3}d\theta = \int_0^{\frac{2\pi}{3}} V_{in}d\theta + \int_{\frac{2\pi}{3}}^{\frac{4\pi}{3}} [V_{in} - V_{m1}\sin(\theta - \frac{2\pi}{3} + \beta_1)]d\theta + \int_{\frac{4\pi}{3}}^{2\pi} [V_{in} + V_{m2}\sin(\theta + \beta_2)]d\theta = 0 \tag{9}$$

$$\rightarrow \begin{cases} V_{m2}\cos(\beta_2-\frac{\pi}{6})+V_{m3}\cos(\beta_3+\frac{\pi}{6})=\frac{2\pi}{\sqrt{3}}V_{in} \\ V_{m3}\cos(\beta_3-\frac{\pi}{6})+V_{m1}\cos(\beta_1+\frac{\pi}{6})=\frac{2\pi}{\sqrt{3}}V_{in} \\ V_{m1}\cos(\beta_1-\frac{\pi}{6})+V_{m2}\cos(\beta_2+\frac{\pi}{6})=\frac{2\pi}{\sqrt{3}}V_{in} \end{cases} \quad (10)$$

TheV_{L1}, $V_{L2}$and$V_{L3}$are voltage of the DC-link inductors (L_1, L_2 and L_3). According to Figure 2, the V_{m1}, V_{m2} and $V_{m3}$are equal to the following values:

$$\begin{cases} V_{m1}=V_{Lr1}-V_{Lr2} \\ V_{m2}=V_{Lr2}-V_{Lr3} \\ V_{m3}=V_{Lr3}-V_{Lr1} \end{cases} \quad (11)$$

V_{Lr1}, V_{Lr2} and V_{Lr3} are the voltage ofthe resonant inductors shown in Figure 2. By solving the equation set (10), the phase-phase voltages are derived as a function of β_1, β_2, β_3 and V_{in}. For the full-bridge inverter, the equation set (10) can be rewritten by employing the inductor volt-second balance principle on$L_d$and considering the following complex equation:

$$V_{m1}\,exp(j\beta_1)+V_{m2}\,exp(j\beta_2-j\frac{2\pi}{3})+V_{m3}\,exp(j\beta_3+j\frac{2\pi}{3})=0\ ,\ \ j=\sqrt{-1} \quad (12)$$

Figure 9 shows the phase-phase voltages of the full-bridge inverter with frequency deviations. In this figure, the resonant frequencies, f_{r1}, f_{r2} and f_{r3} are 25 kHz, 26.5 kHz and 25 kHz, respectively (+6% deviations for f_{r2}). The quality factor of each resonant tank is approximately 20 and the DC-link voltage, V_{in}, is 50 V. In Figure 9(a), a conventional PLL tracks the resonant frequency of f_{r2} at steady state condition, hence the switching frequency is 26.5 kHz.

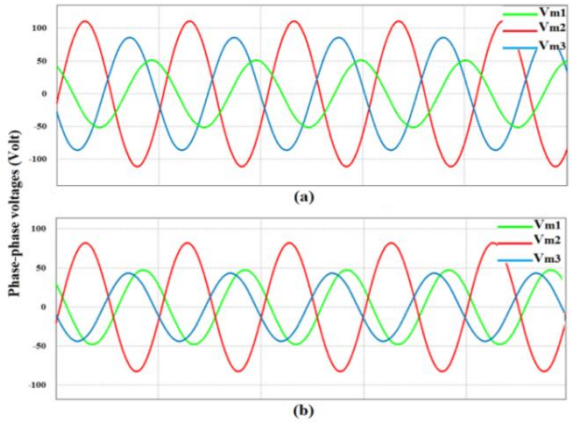


Figure 9

Phase-phase voltage of full bridge parallel resonant inverter: (a) the switching frequency is 26.5 kHz; (b) the switching frequency is 25.5 kHz

Figure 9(b) shows the phase-phase voltages of the full-bridge inverter with the same tolerances. In Figure 9(b), the PLL tracks the average value of the three resonant frequencies, 25.5 kHz, by using the proposed PLL.

Comparing Figure 9(a) and Figure 9(b), it can be concluded that the voltage stress of the inverter is reduced by 20% when the switching frequency is equal to the average value of the resonant frequencies, 25.5 kHz. Hence, for high quality factor (or light-load) conditions (Q>5), the voltage stress of the inverter is significant when the resonant inverter tuning is based on single-phase tuning or conventional PD's.

It can be proven that the minimum value of the voltage stresses occurs when the equation (13) is satisfied. The equation (13) shows a condition that the switching frequency is set to the average value of the resonant frequencies. In the next section, this condition and the performance of the proposed PLL are described in more details.

$$min\{max(V_{m1},V_{m2},V_{m3})\} \Leftrightarrow \beta_1+\beta_2+\beta_3=0 \tag{13}$$

Without loss of generality, consider that the switching frequency of the inverter is tuned by using a conventional PLL that tracks the resonant frequency of f_{r1}. Regarding equations (10) through (13), there is extra voltage stress. The extra stress is maximum for nonsymmetrical tolerances (e.g. ±0 %, ±0 % and ±6 %), and is minimum for symmetrical tolerances (e.g. +3%, -3% and ±0%). The voltage stress increases the current ripples of the DC-link inductor and decreases the net efficiency. The extra voltage stress is suppressed by using the proposed method, which satisfies the equation (13).

Figure 10 shows the stress reduction (in percentage) of the proposed technique for different quality factors and for nonsymmetrical and symmetrical tolerances. Figure 11 shows the voltage of the DC-link inductorwhen the full-bridge inverter is tuned by the conventional and proposed methods at quality factor of about 10 and nonsymmetrical tolerances. Regarding Figure 10 and Figure 11, the DC-link ripples are more affected by the voltage stress for a specific quality factor and frequency deviation.

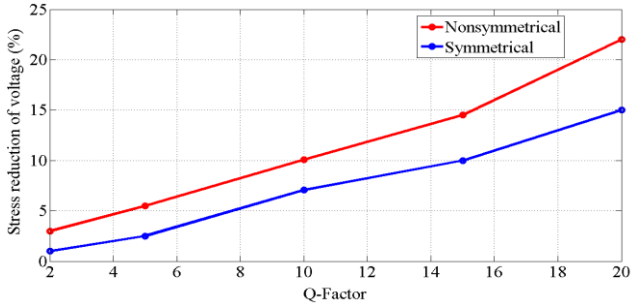


Figure 10

Percentage of stress reduction for the symmetrical and nonsymmetrical tolerances

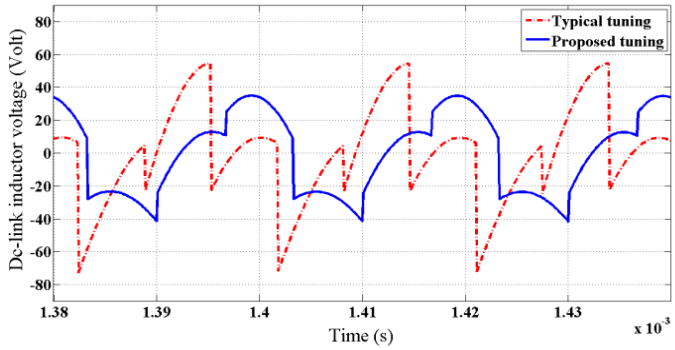


Figure 11

Voltage of DC-link inductor for the proposed and conventional techniques at quality factor of 10 for the full-bridge topology

Forlow quality factors, the system approximately works like a balanced three-phase system because the phase deviations are negligible, see Figure 8(b) and equation set (10). However, the switching frequency should be equal to the average value of the resonant frequencies to minimize the switching losses, negative sequences and DC-link current ripples.

3 The Proposed Resonant Inverter Tuning

PLL circuit consists of a Voltage Controlled Oscillator (VCO), Phase Detector (PD) and a Loop Filter (LF). There are three important parameters for a PLL circuit: VCO's gain K_V, center frequency f_c and LF parameters [25]. In this paper, the LFs are *RC* filterswith time constant of τ.

A three-phase PD is proposed which only uses the voltage of the switches and has no current sensor in the tuning loop. The PD directly connects to LF units to build a Multiplier PD mode [23-25]. To construct the three-phase PD, voltages of S_1, S_2, and S_3 (V_{S1}, V_{S2} and V_{S3}) are passed through comparators and then connected to a logic circuit to produce the phase error signals. According to comparators, the voltage of the switches are saturated in both positive and negative values to produce V_{S1+}, V_{S1-}, V_{S2+}, V_{S2-}, V_{S3+} and V_{S3-}. Figure 12(a) shows waveforms of V_{S1}, $V_{S1-}$and V_{S1+} when the inverter works at over the resonant frequency. Figure 12(b) and 12(c) show the voltage of the switches at over and under the resonant frequency for thehalf-bridge inverter and input voltage of 25 V.

Regarding Figure 12, the phase differences (β_1, β_2 and β_3) aresimplyproduced by using AND gates. For instance, to produce the β_1 when the inverter works at over the resonant frequency (or $\beta_1 < 0$),V_{S1-} and V_{S3+} are the inputs of the AND gate, see Figure 12(b).

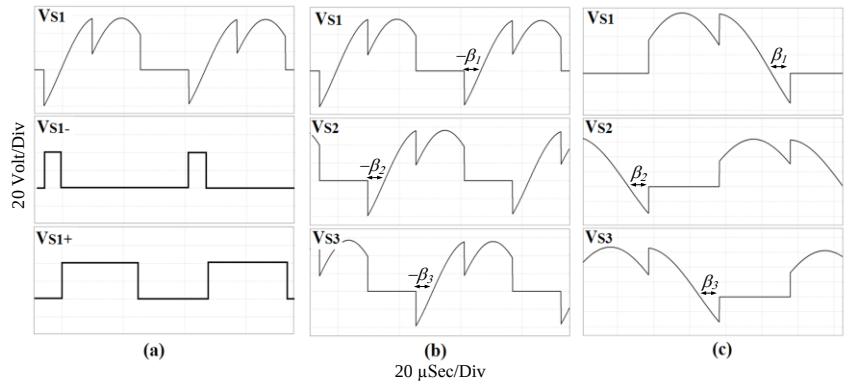


Figure 12

Switches' voltages: (a) voltage of S_1 and its positive and negative duration; (b) voltage of switches at over the resonant frequency; (c) voltage of switches at under the resonant frequency

Equation (14) shows the relationships between β_1 and voltage of the switches. The output of the AND gates are passed through Loop Filters (LF) to remove high frequency components.

$$\begin{cases} x_1 = V_{S1-} \,\&\, V_{S3+} = \beta_1 & , \quad \beta_1 < 0 \\ x_1 = V_{S1-} \,\&\, V_{S3+} = 0 & , \quad \beta_1 \geq 0 \\ x_2 = V_{S1-} \,\&\, V_{S2+} = 0 & , \quad \beta_1 \leq 0 \\ x_2 = V_{S1-} \,\&\, V_{S2+} = \beta_1 & , \quad \beta_1 > 0 \end{cases} \rightarrow \beta_1 = x_2 - x_1 \tag{14}$$

To produce the three-phase PD signals, there are six AND signals,$x_1 \ldots x_6$, which are implemented to produce the phase differences as follows:

$$\begin{cases} x_1 = V_{S1-} \,\&\, V_{S3+} \,,\, x_2 = V_{S1-} \,\&\, V_{S2+} & for\ \beta_1 \\ x_3 = V_{S2-} \,\&\, V_{S1+} \,,\, x_4 = V_{S2-} \,\&\, V_{S3+} & for\ \beta_2 \\ x_5 = V_{S3-} \,\&\, V_{S2+} \,,\, x_6 = V_{S3-} \,\&\, V_{S1+} & for\ \beta_3 \end{cases} \tag{15}$$

According to (15) and Figure 12, the output of phase detector, α is derived as follows:

$$\alpha = (\beta_1 + \beta_2 + \beta_3) = [(x_2 + x_4 + x_6) - (x_1 + x_3 + x_5)] \tag{16}$$

Figure 13 shows the proposed PD circuit with VCO and LF units. To analyze the performance of the PLL, the phase plot of thetank circuits must be linearized at their resonant frequencies as follows [21-23].

$$K_{\beta i} = -\frac{\partial \beta_i (j2\pi f)}{\partial f}\Big|_{f=f_{ri}} \tag{17}$$

The $K_{\beta 1}$, $K_{\beta 2}$ and $K_{\beta 3}$ are the slope of the phase curves near their resonant frequencies in rad/Hz. According to Figure 8 and considering that the deviations are below 3%, theslopes are similar for $|\beta_i| < 30^0$.

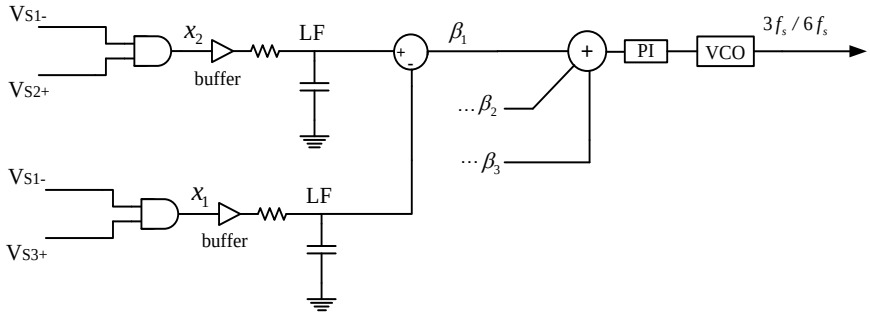


Figure 13
The proposed three-phase PD with VCO and LF units

$$\rightarrow \boldsymbol{K_{\beta 1} = K_{\beta 2} = K_{\beta 3} = K_{\beta}}$$

Therefore, the phase differencescan be derived by equation (18) as follows:

$$\begin{aligned} \beta_1 &= K_\beta (f_{r1} - f_s) \\ \beta_2 &= K_\beta (f_{r2} - f_s) \\ \beta_3 &= K_\beta (f_{r3} - f_s) \end{aligned} \tag{18}$$

The f_s is the switching frequency of the inverter. Hence, the equation (16) is rewritten as follows:

$$\alpha = K_\beta (f_{r1} + f_{r2} + f_{r3}) - 3K_\beta f_s \tag{19}$$

At steady state condition, α isapproximately zero and hence, the switching frequency is derived as follows:

$$\alpha \to 0 \Leftrightarrow f_s = \frac{(f_{r1} + f_{r2} + f_{r3})}{3} \tag{20}$$

By designing a proper PI controller, αis close to zero at steady state condition. According to (20), the proposed PLL tracks the average value of the resonant frequencies. As seen from Figure 14, the output of the PD is passed through the PI controller. The output of the controller is connected to the VCO unit. According to Figure 12 and equation (16), it is worth noting that the high frequency component of the proposed PD is six times the switching frequency (or three times the conventional PD's) [21-25]. Therefore, the proposed method has fast dynamics and the tuning process occurs in less cycles.

Due to three-pulse and six-pulse operation of the half-bridge and full-bridge inverters, the center frequency of the PLL must be close to three times and six times of the resonant frequency. Figure 14 shows the switching sequences for 120^0 conduction mode for full-bridge and half-bridge topologies. Finally, the output of the VCO is connected to a sequential circuit to produce the proper switching sequences.

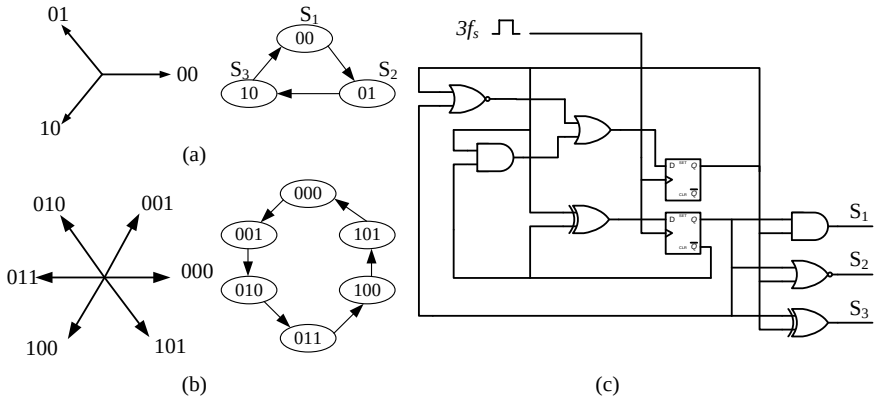


Figure 14

(a) The three-step performance of sequential circuitfor half-bridge inverter; (b) six-step performance of sequential circuitfor full-bridge inverter; (c) the sequential circuit used for half-bridge inverter

Figure 14(c) shows the proposed sequential circuit for the half-bridge topology. To show the PLL dynamics, simulation results are carried out by PSIM simulator for the half-bridge topology. The parameters of the inverter and the PLL are listed in Table 1. Figure 15(a) shows the voltage of $S_1$and the PLL dynamics at start-up. Figure 15(b) shows output signal of the phase detector controller (or input signal of the VCO unit) at start-up. In these figures, the center frequency f_c of the PLL is 65 kHz, which is approximately three times the resonant frequency. According to the resonant frequency, the final frequency of the VCO unit is close to 66 kHz.

In this simulation, the tolerances are less than 3% and the average value of the resonant frequencies is about 22 kHz. The parameters of the PI controller are set to achieve better dynamics. This simulation is done without power regulator. However, by using a power regulator, the voltage stresses of the switches are significantly reduced at start-up,as in [24]. As seen from Figure 15, the output voltage of the controller has three steps for each switching period, which is three times faster thanconventional PD's [21-25].

Table 1

Simulation parameters

Resonant tank parameters		Inverter Parameters		PLL specifications	
C_r	330nF	$L_{1,2,3}$	600μH	f_c	65 kHz
Q	≈ 5	V_{in}	50V	$\frac{P}{I}$	K_I= 5.5×10^4, K_P = 20
L_r	150μH	-	-	τ	330μSec
f_r	≈ 22 kHz	-	-	K_V	1000 (Hz/Volt)

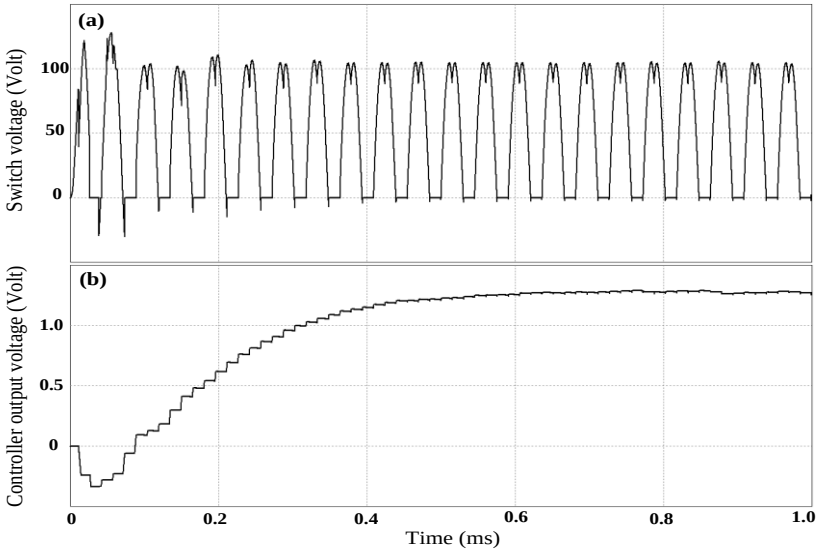


Figure 15

(a) Voltage of S_1 at start-up condition; (b) output signal of the PI controller at start-up condition

4 Experimental Results

A half-bridge inverterwas built and the performance of the inverter with the new PLL was investigated with operating frequency of 22 kHz. As mentioned, the structure of the PDis similar for the full-bridge and half-bridge inverters and the half-bridge topology is implementedfor simplicity. The parameters of the inverter and the PLL are listed in Table 2. In this prototype, the quality factor of the resonant tanks is investigated for 20 and 3. The quality factor of 20 is considered for the no-load condition. The center frequency of VCO is about 65 kHz for operating frequency of about 22 kHz.

Tolerance of theresonant inductor, L_r, is less than 1% and the resonant capacitors are metalized polypropylene film capacitor with maximum tolerance of 5%. Therefore, according to (6), the maximum frequency deviationis less than 3% for each resonant tank. In this prototype, the equivalent load resistances are in series with resonant inductors for mentioned quality factors.

Figure 16(a) shows the performance of the new PLL at start-up condition. In this figure, the PLL's center frequency is 65 kHz, which is approximately three times the average value of the resonant frequencies. The steady state switching frequency (or averaged value of three resonant frequencies) is about 22 kHz at quality factor of 20.

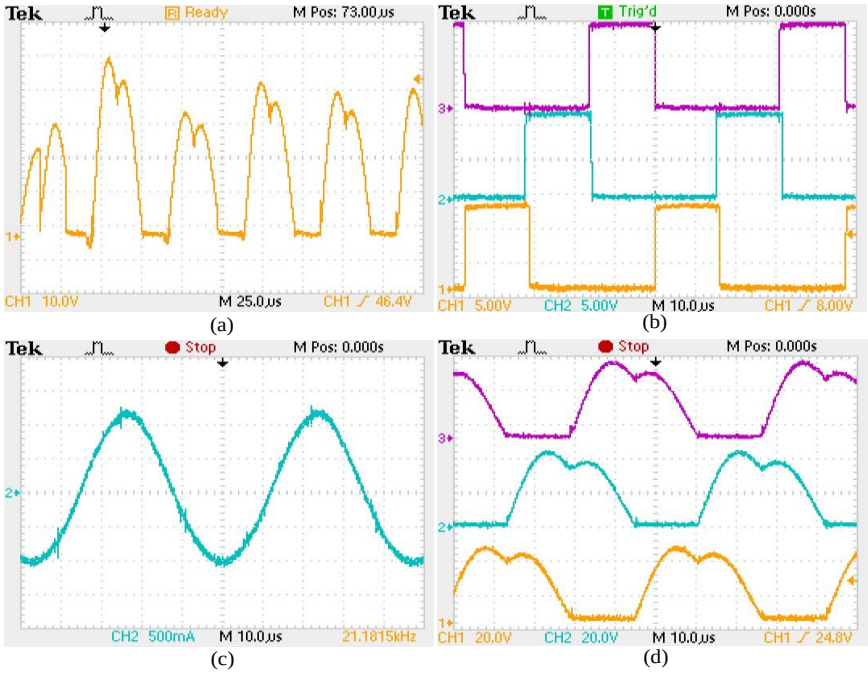


Figure 16

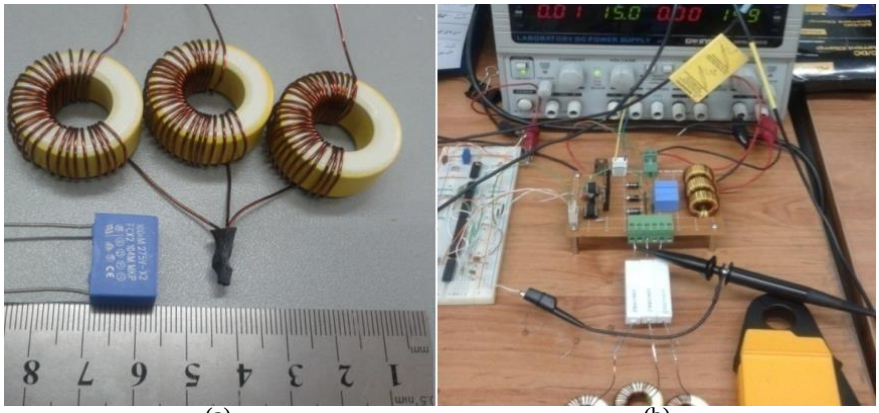
(a) Voltage of S_1 at start-up condition by using the proposed tuning loop and input voltage of 20 V (10 volt/div); (b) gate to source voltage of the switches, (5 volt/div); (c) resonant tank current at quality factor of about 3, (500mA/div); (d) voltage of the switches at steady state condition and input voltage of 20 V and quality factor of about 3, (20 volt/div)

Table 2

Inverter and PLL parameters

Load parameters		Inverter Parameters		PLL specifications	
C_r	≈ 330 nF	$L_{1,2,3}$	600 µH	f_{center}	≈ 65 kHz
Q	≈ 20 and 3	*Series diodes*	BY399	PI	$K_I \approx 6\times10^4$, $K_P \approx 15$
L_r	≈ 150 µH	Switches	IRFP540	τ	1000 µSec
f_r	≈ 22 kHz	Gate drivers	ICL7667	K_V	1000 (Hz/Volt)

The PI controller of the PLL circuit is designed to achieve minimum phase error at steady state condition while the transient response is suitable. The optimum parameters of the PI controller are listed in Table 2. Figure 16(b) and (d) show the gating signals and the voltage of the switches at quality factor of about 3 with 3% deviation. Figure 16(c) shows resonant tank current connected to S_1 at the quality factor of 3 and output power of about 50 W. Figure 17 shows the laboratory prototype of the current source parallel resonant half-bridge inverterwith the resonant inductors and capacitors.



(a) (b)

Figure 17

(a) The three resonant inductors and the resonant capacitor; (b) laboratory prototype of the current source parallel resonant half-bridge inverter

Conclusion

In this paper, a new PLL circuit is proposed for three-phase current source parallel resonant inverters. The new PLL tracks the average value of three resonant frequencies according to the new phase detector performance. This helps to achieve less voltage stresses on the switches and lower distortions in DC-link current. The PLL is investigated in multiplier phase and frequency mode to achieve fast dynamics at transients. The new tuning circuit uses only the voltage of the switches to detect the phase error and there is no feedback from the load currents. Therefore, the circuit is simple, more reliable and cost effective. The new PLL can be used for both full-bridge and half-bridge topologies while the sequential circuit difference must be taken in consideration.

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