Phase-locked Loop Based on Integrating Scanning Conversion

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Abstract: A new principle for developing a phase-locked loop (PLL) based on integrating scan conversion is proposed. The PLL is a nonlinear pulse system based on the closed structure of an integrating scanning converter (ISC) operating in the mode of external synchronization with circuit voltage frequency. The block diagrams, the waveform diagram and frequency synchronization conditions for integrating scanning converter switch by outer signals – bipolar rectangle and harmonic, are provided. The recommendations for choosing the frequency ratio of self-oscillations of the scanning converter and circuit voltage frequency were tested. It is shown that the integrating PLL fully adapts to amplitude instability and circuit voltage frequency within the range of ±50% and higher. Unlike the existing PLLs, the proposed system is a first-order adaptive filter, whose bandwidth is automatically tuned to the amplitude and frequency of circuit voltage. This property of the integrating PLL allows suppressing higher harmonics in the supply circuit with frequency instability within the range of ±50% and higher. The system's high noise immunity to commutation distortions of circuit voltage is also shown. These results show the practicability of using it in semiconductor converter control systems, which receive power from an independent low-power supply system, for example, diesel or wind power generating plants. The limits of the dynamic parameters of this system for gradual change of amplitude and circuit voltage frequency have been determined. A three-phase reverse thyristor rectifier is used as an example of a crossed synchronization flow-chart. The recommendations on choosing the parameters of the integrating PLL and also the results of the practical application of the synchronizing unit as a part of semiconductor converter control systems are provided.

Keywords: control system; integrator; scanning converter; semiconductor converter; phase-locked loop

1 Introduction

Modern electric energy systems performed on a stationary basis (and on an autonomous basis as well) are characterized by a high level of distortion with parameters which are difficult to predict, and which often go beyond distortion

standards and which act as destabilizing factors in the performance of not only the semiconductor inverters, but the control system in general [1-3]. This is why development of a semiconductor converter (SC) control system that is capable of full adaptation to changes in circuit parameters (amplitude, frequency, higher harmonics, commutation and impulse distortions) in addition to high noise immunity is an important issue directed towards improving the performance reliability of the entire electro-technical equipment complexes of industrial plants. Creating such a system is important for application not only to development in the SC area, but to working equipment, in need of overhaul, as well.

The most important element of any SC control system is the synchronizing units (SU) since the accuracy of the control system's synchronization with the supply circuit depends on its operation. In the majority of cases, the SU is out of the closed control loop of the SC control system, and therefore any destabilizing effect of circuit voltage leads to a deviation of its output characteristics. If the supply power is high (minimum distortion and stable circuit parameters), it is usually possible to obtain a stable undistorted synchronization signal without any problems. However, in the case of low-power supply, it is quite a challenge to obtain an undistorted synchronization signal since it must exactly match the phase of the first harmonic of circuit voltage.

The first synchronizing units were designed in accordance with the open circuit principle and were represented by cascade connection of the smoothing filter (for example, aperiodic first-order and relay element with switching thresholds which have a relative asymmetry level of zero) [4]. The disadvantage of this type of SUs is apparent – the defined angle of synchronization fundamentally changes as the amplitude is alternated [5], which affects the SC characteristics in general, and can lead to emergency shutdown.

The application of band-pass filters [6], which detect the useful component of the frequency of zero-phase shift circuit voltage, can be useful when the SC operates in a low-power circuit. However, the main disadvantage of these devices is that they generate noncharacteristic harmonics, which cause problems of harmonic instability. Therefore, we had to discard the use of band-pass filters in the SC control systems.

The development of synchronizing circuitry in view of the above-mentioned disadvantages contributed to the design of closed synchronizing units based on the principle of a phase-locked loop [7-9].

The simplest PLL system consists of an error detector based on a multiplier, a low-pass filter (LPF), a proportional-integral controller (PI), and a voltage controlled oscillator (VCO) (Fig. 1a) [7]. In this PLL, the error signal u_{ERR} in phase and frequency is generated as a result of multiplying the synchronizing voltage $X_S(t) = t \cdot \sin(\omega_1 t + \theta_1)$ and the feedback signal $t \cdot \cos(\omega_2 t + \theta_2)$ and is equal to

$$u_{ERR} = 0{,}5 \cdot \sin[(\omega_1 - \omega_2) \cdot t + (\theta_1 - \theta_2)] + 0{,}5 \cdot \sin[(\omega_1 + \omega_2) \cdot t + (\theta_1 + \theta_2)] \quad (1)$$

The steady-state synchronizing voltage $X_S(t)$ is equal to the feedback signal. In this case, $\omega_1 = \omega_2$ and $\theta_1 = \theta_2$, therefore the first term in expression (1) equals zero. The second steady-state term represents an uncontrolled component with the frequency 2ω. To detect the error signal of the constant voltage u_F and to eliminate the uncontrolled variable component, a low-pass filter (LPF) with a transfer function $W(p) = 1/(T_F p + 1)$ is used. The output signal of the PI-controller $\Delta\omega$ $\Delta\omega$ and the initial frequency ω_0 are used to modulate the frequency and phase of the rotation angle θ, as well as the formation of $\sin(\omega t)$ and $\cos(\omega t)$ at the output of the sinusoidal oscillator (SO).

The disadvantage of the conventional PLL is that it does not provide precise synchronization with the synchronizing signal $X_S(t)$ when its frequency varies within a wide frequency range, for example, when the frequency deviates from the steady-state value within the range of ±50% and higher. This is explained by the fact that the LPF cutoff frequency and the PI-controller parameters have fixed values and are tuned to the initial frequency ω_0.

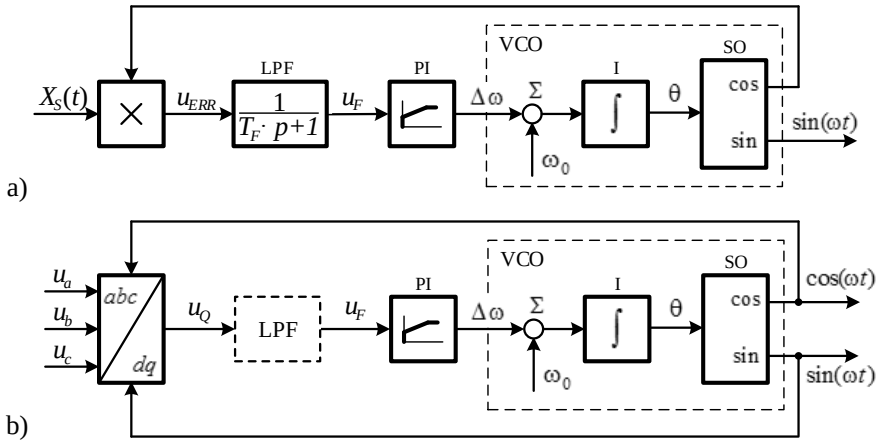

Figure 1

PLL block diagram: conventional (a); based on the *p-q* theory (b)

The PLL system based on the *p-q* theory (Fig. 1b) eliminates this disadvantage [8-9]. The system functions on the basis of the well-known property of the Park-Gorev transform [10], which converts a three-phase coordinate system *abc* into a rectangular synchronous *dq* one. Thus, an error signal $u_{ERR} = u_Q$, corresponding to the difference in frequency and phase between the supply circuit voltage and the feedback signals $\sin(\omega t)$ and $\cos(\omega t)$, is generated at the output of the coordinate conversion unit. In other respects, the composition of blocks and the operation principle of the PLL circuit (Fig. 1b) completely coincide with those of the conventional PLL (Fig. 1a).

The main difference between the conventional PLL and the PLL based on the *p-q* theory is that there is a higher 2nd harmonic in the error signal u_{ERR} of the conventional PLL and the closed loop must allow for an LPF under normal operating conditions. At the same time, the PLL error signal u_Q (Fig. 1b) lacks such component of alternating voltage, so an LPF is not required.

However, if the power bus voltage contains higher harmonics, for example, the 3rd one, then the error signal u_Q will contain the 2nd voltage harmonic. In order to suppress it, an LPF (Fig. 1b) has to be integrated into the PLL system based on the *p-q* theory. And if the supply circuit frequency is unstable within the wide frequency range (±50% and higher), it will be necessary to reconfigure the LPF and the PI-controller so that the PLL can achieve high synchronizing accuracy and stability of its closed loop.

The above-mentioned problem is solved in the PLL based on integrating scan conversion [11]. Hereinafter, this system will be simply referred to as "integrating PLL".

The original contribution of the article is that it proposes a new principle for developing a PLL on the basis of integrating scan conversion, which differs from the existing PLL structures by the ability to suppress higher harmonics in the power supply circuit with frequency instability being within the range of ±50% and above.

Numerous studies conducted by the authors showed that applying the methods of integrating scanning conversion for designing both synchronizing units and semiconductor inverter control systems on the whole is one of the most effective ways of improving their noise immunity, the static and dynamic accuracy [12-16].

The next sections describe an integrating phase-locked loop [11], which combines high noise immunity to circuit distortions (higher harmonics and commutation notches) and an ability to adapt to the oscillation of amplitude and power voltage frequency in a wide range.

2 Static and Dynamic Characteristics of the Integrating PLL

In the core of the integrating PLL lies a continuous structure of an integrating scanning converter with pulse-frequency-width modulation (PFWM) [13, 16], which consists of adders Σ1–Σ2, an integrator I and a relay element (RE) with a hysteresis loop (fig. 1a) of 'zero' relative symmetry and which works in outer synchronization with the supply-line voltage mode [13].

A synchronization signal $X_S(t)$ (a supply-line voltage), which has a sine wave form (Fig. 2b) or a rectangle of bipolar impulses with an average value of zero,

needs to be supplied to the integrating scanning converter (ISC) input for conversion of ISC from the PFWM mode to the forced switch mode, when the pulse-width modulation is being implemented. As a result, the alternating impulses $Y(t)$ with the supply-line voltage frequency of $(T_S)^{-1} = (T_0)^{-1}$, which are shifted by the relatively $X_S(t)$ signal to the angle of synchronization α_S (Fig. 2b, c), reach a steady state on the ISC output. The output integrator signal is proximal by form to the harmonic signal $X_S(t)$. Switching of RE is being executed in achieving a switching threshold $\pm b$ EL by an evolvent of integrator $Y_I(t)$ (Fig. 2c).

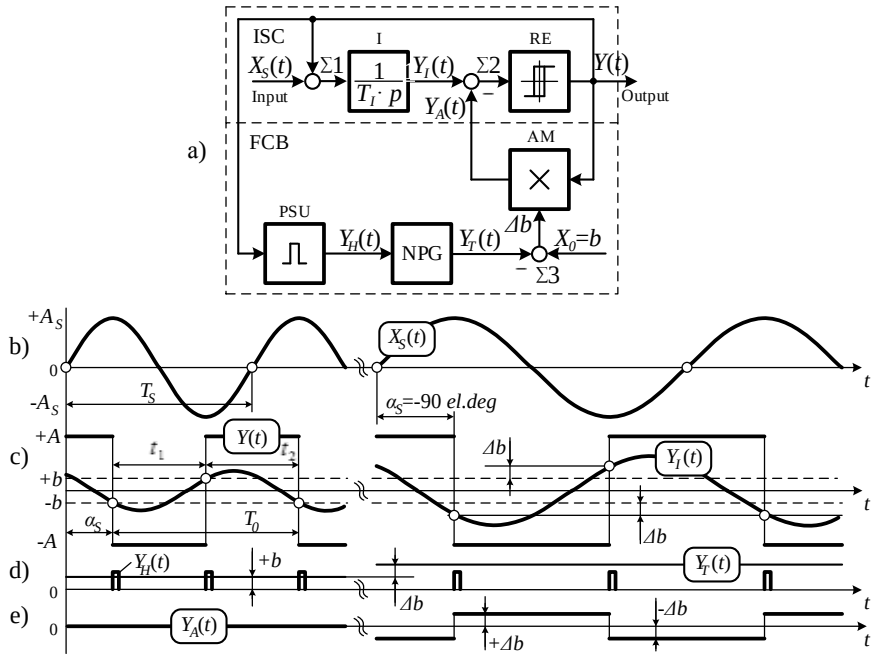

Figure 2
Block diagram of the integrating PLL (a) and waveform diagrams of its signals (b-e)

Conditions for ISC synchronization by rectangle bipolar pulses and harmonic signal are described by the following inequalities:

$$\bar{A}_S \geq |\bar{T}_0 - 1| \tag{2}$$

$$\bar{A}_S \geq 0{,}5\pi \cdot |\bar{T}_0 - 1| \tag{3}$$

In these inequalities $\bar{A}_S = |A_S/A|$ is the scaled amplitude of the A_S synchronization signal (degree of synchronization); $\bar{T}_0 = T_0/T_S$ is the scaled value of the ISC self-auto-oscillation $T_0 = 4\overline{b} \cdot T_I$, when $A_S = 0$, in relation to T_S the period of the synchronization signal $X_S(t)$; $\bar{b} = |b/A|$ is the scaled value of the switching threshold of the RE; $\pm A$ is the amplitude of RE output pulses; T_I is the ISC time constant.

Analysis of equations (2), (3) leads to the following conclusions:

– while $\bar{T}_0 \ll 1{,}0$, the depth of ISC synchronization by rectangle pulses should be chosen considering the $\bar{A}_S \geq 1{,}0$ constraint, and $\bar{A}_S \geq \pi/2$ for the harmonic signal. Otherwise, ISC switches to the self-oscillation mode with the frequency $f = (1 - \bar{A}_S^2)/4\bar{b} \cdot T_I$;

– while $\bar{T}_0 > 1{,}0$, the level of $\bar{A}_S$, required for ISC synchronization by rectangle pulses, as well as by harmonic signal, rises steeply. It is explained by the fact that in order to synchronize the ISC of low undamped frequency $(T_0)^{-1}$ by high frequency synchronization signal with the frequency of $(T_S)^{-1}$, $\bar{A}_S$ needs to be increased in such a way that the equation for second-volt area module $(S_S = |A_S \cdot T_S|) > (S = |A \cdot T_0|)$ is exactly satisfied. Otherwise, the pulse frequency $(T_0)^{-1}$on the ISC output is less than the frequency$(T_S)^{-1}$ of $X_S(t)$ synchronization signal;

– while $\bar{T}_0 = 1{,}0$, the $\bar{A}_S$ is approaching zero, which is why choosing the self-oscillation frequency $(T_0)^{-1}$ of ISC equal to the frequency $(T_S)^{-1}$ of synchronization influence $X_S(t)$ is appropriate.

The phase shift α_S, between the synchronization influence $X_S(t)$ and input impulse $Y(t)$ (Fig. 2b, c), depends on the scaled value of self-oscillation period $\bar{T}_0 = T_0/T_S$ and the depth of synchronization $\bar{A}_S$

$$\alpha_S = -90el.deg. \cdot \left[\!\left[1 + \frac{\bar{T}_0 - 1}{\bar{A}_S}\right]\!\right]. \quad (4)$$

Equation (4) shows that while $\bar{T}_0 = 1{,}0$, the ISC self-oscillation frequency $(\bar{T}_0)^{-1} = 1/4\overline{b} \cdot T_I$ equals the signal frequency $(T_S)^{-1}$ of synchronization $X_S(t)$ and $\bar{A}_S$ has any value, the synchronization angle α_S always stays constant and equals –90 el. deg. This gives the integrating PLL the properties for adaptation to instability of circuit voltage amplitude within the range of ±50 % and higher, which provides the basis of the space of static state $\Delta\bar{\alpha}_S = f(\Delta\bar{A}_S, \bar{A}_S)$ (Fig. 3a) derived from *MatLab+Simulink* simulation of the integrating PLL with the change in synchronization depth within the range $0{,}25 \leq \bar{A}_S \leq 10{,}0$. In this equation $\Delta\bar{\alpha}_S = (\alpha_S{}^* / \alpha_S) - 1$ is the scaled error of synchronization angle $\alpha_S{}^*$ in relation to the anterior synchronization angle α_S as the outer distortion is absent, and which possesses a value of -90 el. deg; $\Delta\bar{A}_S = (A_S / A_{S.N}) - 1$, $\Delta\bar{f}_S = (f_S / f_{S.N}) - 1$ are the scaled errors of amplitude A_S and frequency f_S of supply-line voltage $X_S(t)$ in relation to their scaled values $A_{S.N}$ and $f_{S.N}$ respectively.

As the frequency $\Delta\bar{f}_S$ and the synchronization signal degree $\bar{A}_S$ change, the area $\Delta\bar{\alpha}_S = f(\Delta\bar{f}_S, \bar{A}_S)$ takes on substantially non-linear pattern (Fig. 3b). Thus, with the increase of $\Delta\bar{f}_S$, the error $\Delta\bar{\alpha}_S$ increases due to the violation of the equality between the ISC self-oscillation frequency $(T_0)^{-1}$ and the supply-line voltage frequency $(T_S)^{-1}$ and according to (4), the synchronization angle α_S deviates from the scaled value equal to -90 el.deg. This is one of the disadvantages of the integrating PLL.

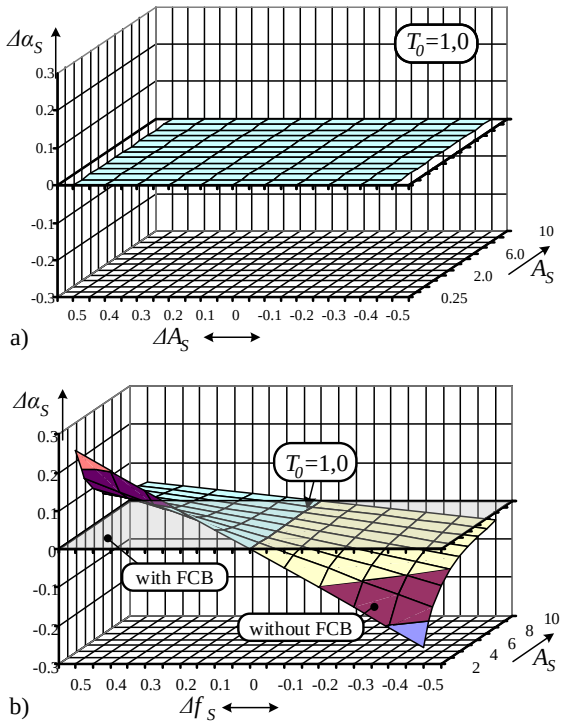

Figure 3

The space of static state $\Delta\bar{\alpha}_S = f(\Delta\bar{A}_S, \bar{A}_S)$ (a) and $\Delta\bar{\alpha}_S = f(\Delta\bar{f}_S, \bar{A}_S)$ (b) of the integrating PLL for outer synchronization by harmonic signal

For elimination of the described disadvantage, a frequency correction block (FCB) is included in the PLL circuit (Fig. 2a). It consists of an amplitude modulator (AM), an adder Σ3, a voltage supply $X_0 = b$, a phase-to-voltage converter (PVC) and a narrow-pulse generator NPG, which starts at the rising and trailing impulse flanks of the ISC output.

At the scaled circuit voltage frequency the signal on the PVC output $Y_T(t)$ equals the ER switching threshold b (Fig. 2d) in absolute value. This is why $Y_A(t)$ equals zero on the AM output (Fig. 2e).

As the circuit voltage frequency $X_S(t)$ oscillates from the scaled value (Fig. 1b), the signal $Y_T(t)$ increases to $(b + \Delta b)$ level on the PVC output (Fig. 2d). An alternating signal $Y_A(t)$ with an amplitude Δb and period that equals period T_0 of the ER output signals, is formed on the AM output (Fig. 2 c, e). This changes the ER switching threshold $|b|$ by $|\Delta b|$, satisfying the equation $T_S = T_0 = 4\overline{b \cdot T_I}$ (Fig. 2 c). As a result, in a steady-state mode, the synchronization angle α_S (between the supply-line voltage $X_S(t)$ and the ISC output pulse) stays -90 el.deg. (Fig. 2 b, c). That is why the synchronization angle error $\Delta\bar{\alpha}_S$ equals zero. This proves the static state area (Fig. 3 b). In these circumstances, when the frequency

correction block is added to the PLL circuit, the circuit voltage frequency range of motion significantly expands from -0.9 to 3.0 (or from 5 to 200 Hz in absolute numbers at the scaled circuit voltage frequency $f_{S.N} = 50Hz$) as the synchronization signal level is $0{,}25 \leq \bar{A}_S \leq 10{,}0$.

To determine the degree of dependence of the ISC dynamic characteristics on the parameters of the synchronizing signal $X_S(t)$, we applied *MatLab + Simulink* software to make the Bode magnitude plot $k = f(\bar{F})$ of the integrating PLL system synchronized by both rectangular and harmonic signals with different values of synchronization depth (Fig. 4). An alternating harmonic signal $X_A(t) = A_A \cdot sin(2\pi f_A t)$ with a constant amplitude $\bar{A}_A = \left|\frac{A_A}{A}\right| = 0{,}1$ and frequency f_A was applied to the ISC input that was also exposed to the synchronizing effect $X_S(t)$. The central component Y_0 of the ISC output pulses was isolated using a digital filter that implements the algorithm $Y_0 = A \cdot (t_2 - t_1)/T_0$. Here, t_1, t_2, T_0 are the time intervals and period of the ISC output pulses (Fig. 2c), and A is its amplitude. In this case, the input signal level $X_A(t)$ and the average value Y_0 of the ISC output pulses get uniquely connected only after the repetition period T_0 of the pulses $Y(t)$ ends.

Fig. 4 uses the following notations: $k = Y_{0.m}/A_A$ is the ISC transmission coefficient; $\bar{F} = f_A/f_S$ is the scaled frequency of the harmonic signal $X_A(t)$ with respect to the frequency f_S of the synchronizing effect $X_S(t)$.

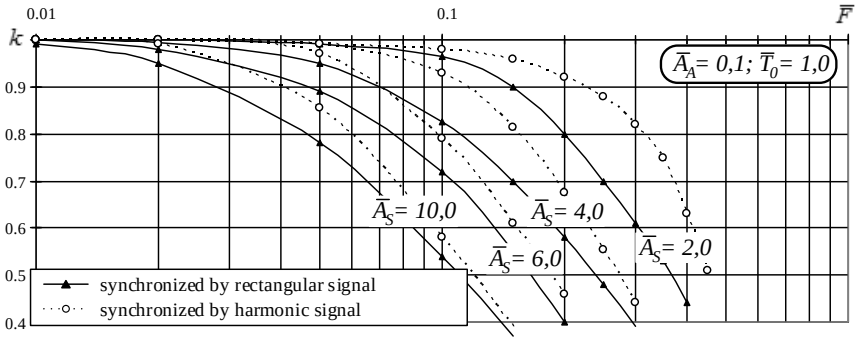

Figure 4

Bode magnitude plot of the integrating PLL with different values of synchronization depth

Analysis of the Bode magnitude plot (Fig. 4) allows us to conclude [17] that the integrating PLL's dynamic properties are close to ones of the first-order aperiodic link $W(p) = 1/(T_E p + 1)$ with the time constants equivalent $T_E \approx 0{,}25\bar{A}_S \cdot T_S$ (5) for synchronization by rectangle pulses and $T_E \approx (\pi \cdot \bar{A}_S \cdot T_S)/16$ (6) for synchronization by harmonic signal.

However, it needs to be considered that this "linearization" is valid for only the $\bar{F} = f_A/f_S \leq 0{,}5$ area of input frequency impact, which is derived from the Kotelnikov theorem [18]. If the frequency is higher, the scanning converter, being

a pulse system, switches to the slow sampling of dynamic input signal mode [13, 19].

– the integrating PLL is an adaptive filter whose parameters readjust into the functions of the amplitude $\bar{A}_S$ and the frequency ${T_S}^{-1}$ of the synchronization signal (of circuit voltage). As a result, the integrating PLL synchronizes with the circuit voltage with high accuracy (the synchronization angle error $\Delta\bar{\alpha}_S$ tends to zero) even if there are higher harmonics in the supply voltage and frequency instability of the synchronizing signal within the range of ±50% and higher. This is confirmed by the results of the integrating PLL simulation when the synchronizing signal $X_S(t)$ has the third lowest-frequency voltage harmonic with the amplitude $\bar{A}_{S(3)} = A_{S(3)}/A_{S(1)}$ that is equal to 30% of the main component amplitude $A_{S(1)}$ of the circuit voltage with two frequency values $f_S = 50\ Hz$ (Fig. 5a) and $f_S = 10\ Hz$ (Fig. 5b) of the supply voltage.

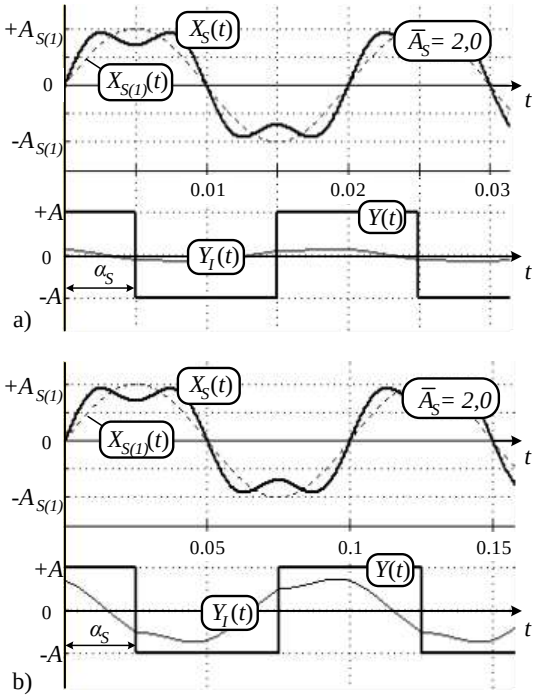

Figure 5

Waveform diagrams of the integrating PLL with the third harmonic in the synchronizing signal and the change in the supply voltage frequency: $f_S = 50\ Hz$ (a) and $f_S = 10\ Hz$ (b)

Fig. 5 shows that the 3rd harmonic is completely suppressed by the integrating PLL, and the synchronization angle α_S is equal to minus 90 el. deg. It is noteworthy that, other things being equal, a synchronization error occurs in the existing PLL systems (Fig. 1) because of the fixed values of the low-pass filter

bandpass and the PI-controller parameters that are tuned to the nominal frequency of the synchronizing voltage;

– representation of the integrating PLL in the form of a first-order aperiodic filter indicates its high noise immunity to commutation and pulse distortions of circuit voltage. This is confirmed by the results of the integrating PLL system simulation when there are commutation notches in circuit voltage that reach the level of $\gamma_C = 25$ el. deg. (Fig. 6a). The notches were created by a three-phase bridge thyristor rectifier of current when it operated for a low-power circuit. In this case, the synchronization angle error was $\Delta\bar{\alpha}_S = 0$ ($\alpha_S = -90$ el. deg.), since commutation notches "1" and "2", "3" and "4" mutually compensated each other in the time intervals t_1 and t_2, or areas S_1', S_1'' and S_2', S_2'' in subintervals t_1', t_1'' and t_2', t_2'' equal each other (Fig. 6b).

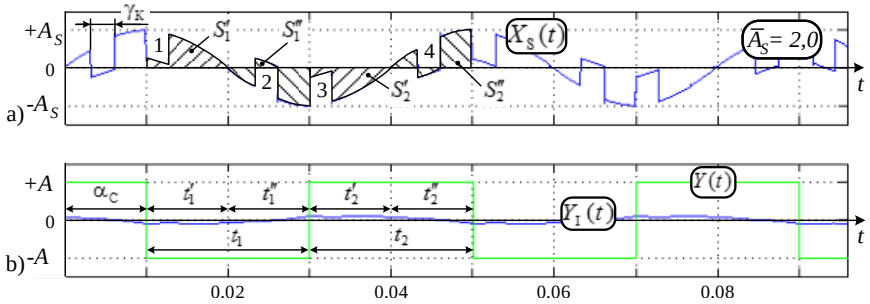

Figure 6

Waveform diagrams of the integrating PLL at commutation notches in circuit voltage ($\gamma_C =$ 25 el. deg.)

In a real industrial environment the over-voltage amplitude and the circuit voltage frequency dips, generally, appear not instantly, but after a certain time interval, which depends on the loading conditions and the type of load included in the circuit. This is the reason why the analysis of the integrating PLL operation in the conditions of the smooth change in amplitude (Fig. 7a) and the frequency (Fig. 7b) of the circuit voltage appears to be of interest.

In Fig. 7 the following notations have been introduced: $\Delta\bar{A}_S$ is the scaled error of an actual circuit voltage amplitude A_S in relation to its rated value $A_{S.N}$; $\bar{S}_U = \Delta A_S / A_{S.N}$ is the scaled velocity of change in amplitude ΔA_S in one period T_S of circuit voltage in relation to its rated amplitude $A_{S.N}$; $S = \frac{(T_S)^{-1} - (T_{S.N})^{-1}}{1sec}$ is the absolute velocity of change in the circuit voltage frequency $(T_S)^{-1}$ in the set time interval t_3 equal to 1 second.

The results of the integrating PLL research have shown that in the dynamic operations the allowed velocity of change in amplitude $\bar{S}_U$ in one circuit voltage period and the frequency S_f makes ±11 % and ±9 Hz/s in 1 second in the conditions when the maximum synchronization angle inclination $\Delta\alpha_S$ does not

transcend ±2 el.deg., and the depth of synchronization is chosen out of the range $\pi/2 \leq \bar{A}_S \leq 8{,}0$ (Fig. 8).

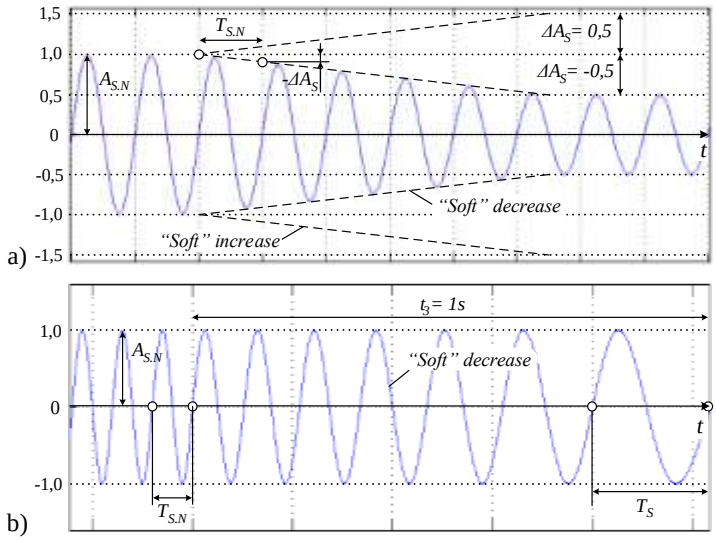

Figure 7

Test impact for analysis of the dynamic characteristics of the integrating PLL at the smooth changes of amplitude (a) and frequency (b) of the circuit voltage

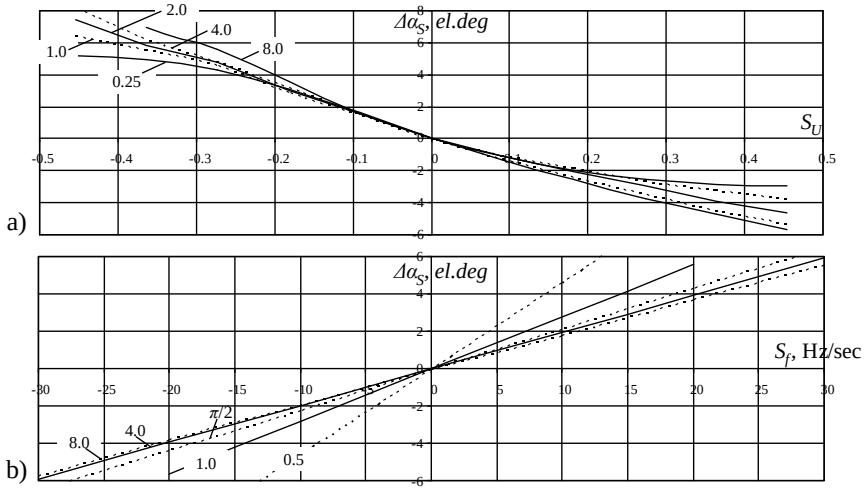

Figure 8

Graphs of dependencies of the absolute synchronization angle error $\Delta\alpha_S = f(\Delta\bar{S}_U)$ (a) and $\Delta\alpha = f(S_f)$ (b) for integrating PLL at different depth of synchronization $\Delta\bar{A}_S$

The optimal level $\bar{A}_S$ is considered to meet the range of $\pi/2 \leq \bar{A}_S \leq 4{,}0$, when the speed of response and the immunity to noise are compromised.

The above results suggest the efficiency of using the integrating PLL in the control systems driven by SC and supplied by autonomous low-power supply systems with a high-level of distortion (higher harmonics and commutation notches) and unstable circuit voltage parameters as well.

Occurrence of the phase shift α_S (equal to -90 el.deg) between the synchronization signal $X_S(t)$ and the output pulses $Y(t)$ (Fig. 2b, c) of the integrating PLL (Fig. 2a) involves an untraditional set-up of the synchronization circuit of the SC control system (CS). One of the set-up options, for example, is the method of CS channel cross synchronization that can be applied in a three-phase thyristor rectifier with a synchronous multichannel control system (Fig. 9a).

Here the PLL-A output sync-pulse (with the duration of 180 el.deg.) outruns phase A by 90 el.deg. (Fig. 9b). Herein the rising flank of this pulse coincides with the natural commutation point of phase C. As a result, the synchronization of the phase C control channel can be done by the PLL-A output sync-pulse. The synchronization of other SC control channels can be done the same way (Fig. 9a).

In order to get the sync-pulses to coincide with the momentum of phase voltages going through the zero point, PLL-A, PLL-B and PLL-C should be synchronized from linear voltages *AB*, *BC* and *CA*, which outrun the phase ones *A*, *B*, *C* by 30 el.deg.

The integrating PLL (Fig. 2a) can be used in the control systems for active voltage (current) rectifiers, active power filters, matrix frequency converters and other SC. These engineering solutions are considered in more detail in the paper [20].

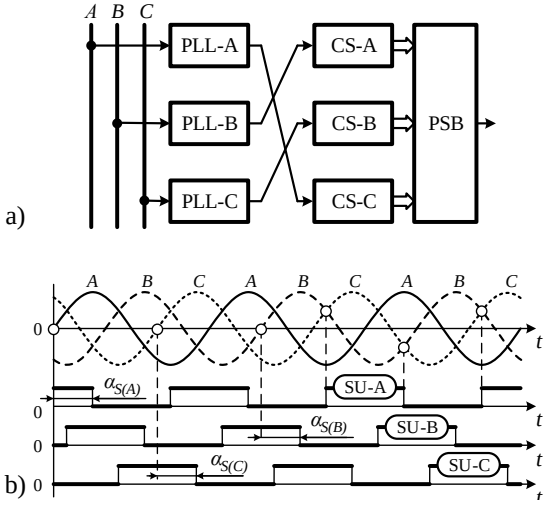

Figure 9

Block diagram (a) and the signal waveform diagram (b) of cross synchronization system of the semiconductor inverter (PLL-A, PLL-B, PLL-C – PLL of phase channels A, B, C; CS-A, CS-B, CS-C – control system for phase channels A, B, C; PSB – power semiconductor block)

Fig. 10 shows the waveform chart of the circuit voltage and the output signal of the integrating PLL system, which functions in the cross-strapping mode (Fig. 9a) in the reverse thyristor rectifier for an electric drive of a direct current control system. The experiment took place on the diesel-generator plant of a drilling rig of the VI group. The total load of the plant was about 90%. Trouble-free performance of an entire technological complex was provided, despite the abnormally high-level of the circuit voltage distortion. This is achieved due to the ISC closed structure and an integrator in its direct control channel. With respect to the synchronizing effect, the system represents a first-order aperiodic filter with an equivalent time constant, which readjusts depending on the circuit voltage parameters.

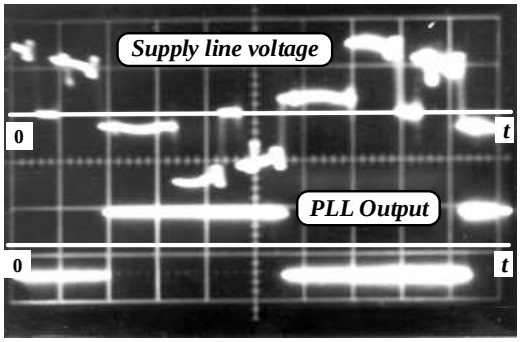

Figure 10

Waveform chart of the circuit voltage and the PLL system output signal in co-operation of several thyristor rectifiers for a low-power supply system

The PLL diagram, showed in Fig. 2a, was also tested on 84 AC thyristor regulators for the soft start of asynchronous electric drives [21] at the JSC "Chelyabinsk Tube-Rolling Plant", and showed high noise immunity and operational reliability.

Conclusions

An analysis of the static and dynamic characteristics of the integrating PLL, based on the integrating scanning conversion has been made. The PLL is a nonlinear impulse system based on the locked structure of an integrating scanning converter (SC) operating in the mode of external synchronization with circuit voltage frequency. It has been determined that for the SC the frequency of self-oscillation should be chosen equal to the scaled synchronization signal frequency. It excludes the drop out of outer synchronization mode of the device in the face of significant circuit voltage failures. At the frequency deviation of the supply voltage the equation listed above is satisfied due to the inclusion of the frequency correction block in the PLL system.

It has been shown that the integrating PLL system fully adapts to the instability of the amplitude and frequency of the circuit voltage within the range ±50% and

higher. Unlike the existing PLL systems, the proposed system is a first-order aperiodic filter $W(p) = 1/(T_E p + 1)$ with the equivalent time constant $T_E \approx (\pi \cdot \bar{A}_S \cdot T_S)/16$ and $T_E \approx 0{,}25\bar{A}_S \cdot T_S$ for the harmonic synchronization signal and the rectangular one) that automatically adjusts depending on the amplitude and frequency of the circuit voltage. This property of the integrating PLL system allows suppressing higher harmonics in the power supply system, while frequency instability is within ±50% and higher. Moreover, the proposed PLL system has high noise immunity to commutation distortions of the circuit voltage. This is achieved due to the closed SC structure and the presence of an integrator in its direct control channel.

Basing on the studies, we have formulated the recommendations on the choice of the integrating PLL system parameters. The optimal level of synchronization depth $\bar{A}_S$ is the range $\pi/2 \leq \bar{A}_S \leq 4{,}0$ where speed and noise immunity are compromised. In dynamic operating modes, the permissible change rate of the amplitude in one circuit voltage period is ±11%, and that of the frequency per one second is ±9 Hz/s, provided that the maximum deviation synchronization angle does not exceed ±2 el. deg, and the synchronization depth is selected according to the condition $\pi/2 \leq \bar{A}_S \leq 8{,}0$.

We have proposed a cross method for synchronizing the channels of SC control systems based on the integrating PLL. We have provided the results of the practical operation of the cross-strapping synchronization being a part of control systems of the reverse thyristor rectifier for a direct current electric drive and thyristor voltage regulator for soft start of asynchronous electric motors, which proved its high noise immunity and operation reliability.

Thus, we recommend that the proposed integrating PLL be used in SC control systems that are supplied by an autonomous low-power supply system with a high-level of distortions (higher harmonics and commutation notches) and unstable circuit voltage parameters.

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